HARDWARE LAB 2

Designing BCD-to-seven-segment decoder

Digital Design: CPEN214

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1. Complete the segments truth table for digits 2 through 7.

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **DIGIT** | **INPUTS** | | | | **OUTPUT (seven segment)** | | | | | | |
| **A** | **B** | **C** | **D** | ***a*** | ***b*** | ***c*** | ***d*** | ***e*** | ***f*** | ***g*** |
| **0** | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| **1** | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| **2** | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| **3** | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| **4** | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| **5** | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| **6** | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| **7** | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

1. Obtain the simplified Boolean expressions in sum-of-products form for all the segments *a 🡪* g. The simplified expression for segment *a* is provided in Fig. 3.
   1. a = B’D’ + C + BD

|  |  |  |  |
| --- | --- | --- | --- |
| * 1 | * 0 | * 1 | * 1 |
| * 0 | * 1 | * 1 | * 1 |

* 1. b = B’ + C’D’ + CD

|  |  |  |  |
| --- | --- | --- | --- |
| * 1 | * 1 | * 1 | * 1 |
| * 1 | * 0 | * 1 | * 0 |

* 1. c = C’ + D + B

|  |  |  |  |
| --- | --- | --- | --- |
| 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 |

* 1. d = B’D’ + CD’ + B’C + BC’D

|  |  |  |  |
| --- | --- | --- | --- |
| * 1 | 0 | 1 | 1 |
| * 0 | 1 | 0 | 1 |

* 1. e = B’D’ + CD’

|  |  |  |  |
| --- | --- | --- | --- |
| * 1 | * 0 | * 0 | * 1 |
| * 0 | * 0 | * 0 | * 1 |

* 1. f = BD’ + C’D’ + BC’

|  |  |  |  |
| --- | --- | --- | --- |
| * 1 | * 0 | * 0 | * 0 |
| * 1 | * 1 | * 0 | 1 |

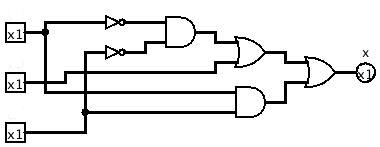
* 1. g = BC’ + CB’ + CD’

|  |  |  |  |
| --- | --- | --- | --- |
| 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |

……

1. Using logic gates, construct the circuits to realize the logic expressions for the necessary segments whose outputs you will use to display any 3 numbers (0 🡪 7). Your circuit should be expandable to display all numbers.

a = B’D’ + C + BD



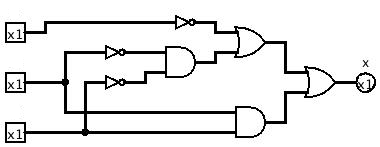
a

D

C

B

b = B’ + C’D’ + CD



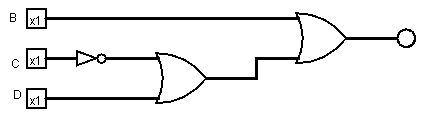
b

B

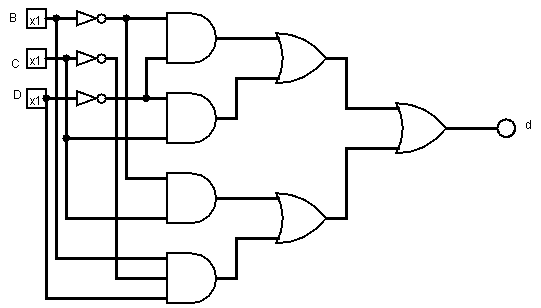
D

C

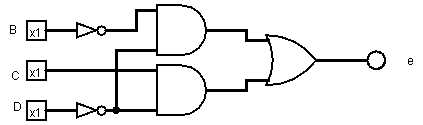
c = C’ + D + B



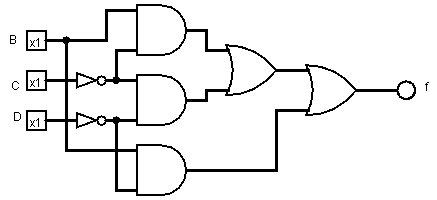
d = B’D’ + CD’ + B’C + BC’D



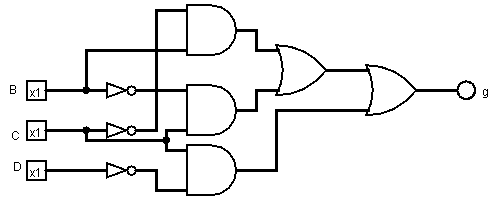
e = B’D’ + CD’



f = BD’ + C’D’ + BC’



g = BC’ + CB’ + CD’



1. For an extra 5 points (NOT 5%) added to the final exam grade, construct the circuit to display (0 🡪 7). Warning: this is a lot of wiring. For an additional 5 points, connect this circuit to the 3-bit synchronous counter output in lab 3.

The typed-up report should include:

1. Completed truth table and K-maps for all segments
2. Circuit diagrams for the segments that you will use

The grading for this lab is as follows: (40% report and 60% demo)

Truth table …………………5%

K-Maps……………………20%

Circuit diagrams…………..15%